

SPASE - 2 Trigger Logic

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Notes:

- Some of the threshold settings are changed
January 2003 Serap Tilav
- Vulcan and its trigger logic wirings are disconnected
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This short report details the trigger configuration of the SPASE-2 array in the Summer season of 1995/1996. The following pages give a comprehensive overview as to how the logic and DAQ was left in February 1996. Figure 0.3 shows a schematic set-up of the trigger logic and signal processing. Virtually every part of the trigger logic was checked and documented, points on the diagram are explained more clearly and expanded upon in the following text.

0.1 SPASE-2 Trigger Logic

1. The D2 output from the splitter passes directly into a LeCroy 428f linear fan-in fan-out NIM module. In total there are eight 428f's used for this purpose. Each is operated in 4x4 mode. The purpose of these modules is to linearly sum photomultiplier signals from detectors within the same station to produce 1 signal per station. For stable operation with 428f it is necessary to use at least two output channels, so whilst one output is fed to the 4413 discriminator the other is terminated 50 Ohm. Beware, there are two things that need to be carefully monitored when using the 428f.
 - On the front panel of the 428f there is a trim potentiometer to remove any d.c. signal level. It is necessary to adjust this to zero.
 - If too many 428fs are placed in the same NIM bin then the power supplied to each 428f may not be great enough. With hindsight, this has most greatly affected the ability to trim any d.c. bias as mentioned above.
2. The LeCroy 4413's discriminators are set to a discrimination level which is -45 mV. This is equivalent to the single particle level and is sometimes referred to as the D2 level. I believe one of these modules belongs the AMANDA and Steve Barwick.
3. The LeCroy 4415 discriminators are modified to accept differential ECL level signals (this is the output level of signals from the 4413s). The purpose of the 4415 is simply to stretch the pulse width as supplied by the 4413 previously. The discrimination level is again set to -45 mV but this is low enough to fire off differential ECL signals whilst not triggering on noise. The output width of these signals was not measured.

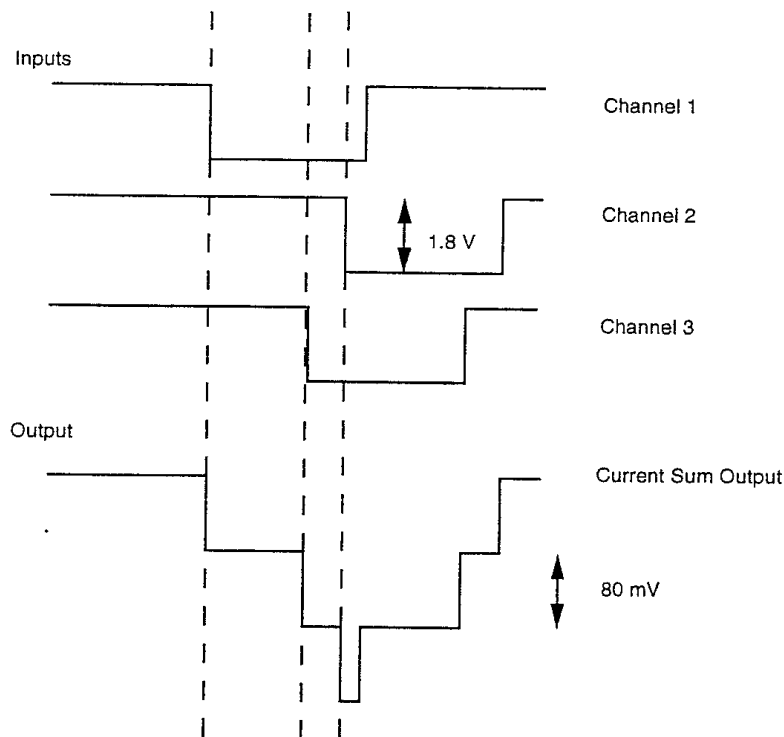


Figure 0.1: Current sum output from 4532 CAMAC module

4. The LeCroy 4434 scalar monitors the D2 rates of each station. This module belongs to AMANDA.
5. The 4532 majority logic unit acts like a coincidence unit. The current sum output from this module drives an 80 mV pulse into a 50 Ohm load. Figure 0.1 shows the current sum output from the 4532 unit for given input signals.
6. The 821 LeCroy discriminator is a NIM module. It discriminates the pulse from the 4532 current sum output. Changing the discrimination level of this module affects the trigger threshold of the array by changing the fold requirements. Currently the 821 is set at -260 mV and produces a 1 μ sec NIM level pulse and triggers at a rate of approximately 8 Hz. Table 0.1 summarises the discriminator ranges for particular fold settings.
7. The output from the 821 discriminator is then passed to LeCroy 222

Lower Threshold	Fold	Upper Threshold
0 mV	1-fold	-80 mV
-80 mV	2-fold	-160 mV
-160 mV	3-fold	-240 mV
-240 mV	4-fold	-320 mV
-320 mV	5-fold	-400 mV
-400 mV	6-fold	-480 mV

Table 0.1: Current sum output from 4532 CAMAC module

Gate generator and delay NIM type module. This produces a NIM level gate 1.5 μ sec in duration. The purpose of the 222 is to extend the pulse width from the 821.

8. The output from the 222 is then fed directly into the veto input of a 365 al coincidence NIM module. This is set for 1-fold coincidences. Thus, the setting of a n-fold pulse as determined by the 4532 MALU and the following 821 discriminator results in fast clears to the TDCs and ADCs being inhibited (veteoed).
9. The 3412 discriminators have a threshold set to -15 mV or 20 DAC counts if programming their threshold from CAMAC. The output width is set to 20 nsec. All these discriminators are operated in remote mode which means that they are controlled via CAMAC and not the front panel potentiometers. The discriminators are programmed to work in burst guard mode.
10. One output from the 3412 is fed directly into the TDCs (2277). The TDCs are operated in common stop and are programmed to latch leading and trailing edges. Coupled with the 3412s being operated in burst guard mode results in the TDC measuring time over threshold (-15 mV) for signals.
11. The second copy of the discriminator outputs is counted by four 4434 scalars. These scalars are free running always. Data are recovered from these modules every 100 minutes.
12. The current sum outputs from the eight 3412's are then fed into an octal 710 discriminator. The 3412 drives a 50 mV signal into a 50 Ohm

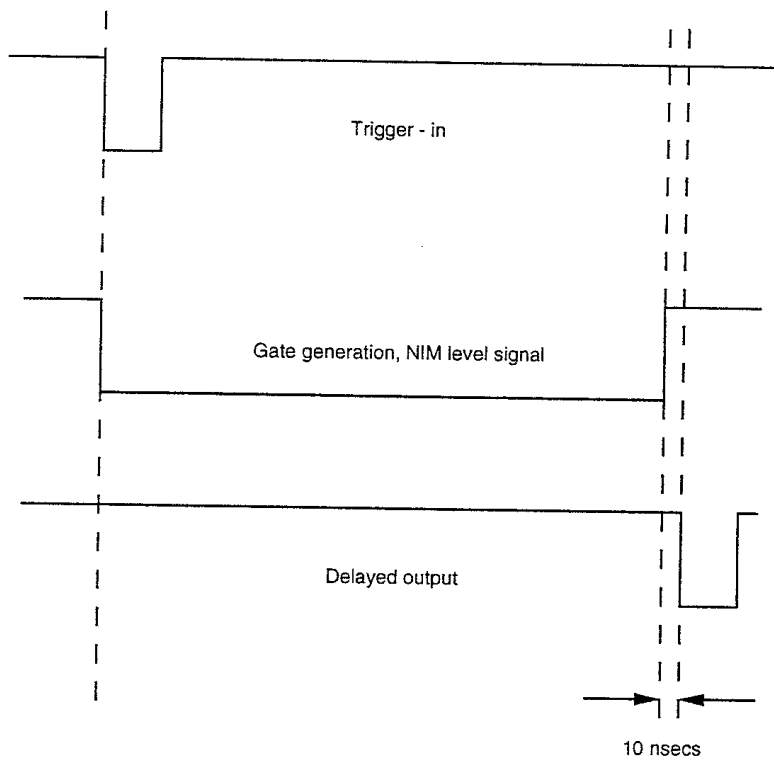


Figure 0.2: Delayed output from 222

load. All channels on the 710 discriminator have their threshold's set at -25 mV. The purpose of the 710 is to sum all the current sums from each 3412 discimiinator and produce a single pulse.

13. The current sum output from the 710 discriminator (50 mV into a 50 Ohm load) is passed to an 821 discriminator whose threshold is -40 mV. Thus it discriminates on each 1-fold D1 trigger from the entire array. The rate of D1 triggers was measured to be 7500 Hz.
14. The output from the 821 is fed into a gate generator and delay module (222) and it produces a gate of width 1.2 μ sec. The gate is used by the ADCs. A delayed output from the 222 of this signal is also used. The timing characteristics of the delayed output are shown in figure 0.2.
15. The delayed output from the 222 is then fed into an 821 dscriminator whose threshold is -170 mV, this is just to discriminate the NIM level signal from the 222. The width is set to 60 nsecs. The purpose of the

821 is to produce two NIM level signals from the delayed output of the 222.

16. One output from the 821 discriminator is passed to a 365 al coincidence unit. The purpose of the 365 al is to decide whether enough n-fold triggers occurred. If not then fast clears are distributed to ADCs and TDCs. NOTE, It has been thoroughly checked that when n-fold triggers occur, the veto pulse is always present when the fast clear pulse (possibility) arrives at the 365 al.
17. The fast clear pulse is distributed to the FERA driver 4301 for subsequent passage to the 4300b ADCS via the ADC command/control bus.
18. The FERA driver is responsible for passing both the fast clears and the gates to the ADCs. This is achieved by daisy chaining the ADCs along the command bus. All ADCs except for the last in the chain have had their termination resistors removed.
19. The TDC fast clear is passed to a 4x4 logic fan-in fan-out to produce four copies of the fast clear.
20. Each copy of the fast clear signal is then input to a 4616 ECL-NIM-ECL level converter.
21. From there each fast clear is distributed individually to each TDC via 100 Ohm twisted pair cable.
22. The second output from the 821 D1-summed fold, is essentially the trigger. It is delayed by 32 nsecs before reaching the 365 al coincidence unit via RG 168 (lemo) cable.
23. The output from the "fast clear" coincidence unit (described in section 8) is only produced if there was not a sufficient n-fold (or D2) trigger. The output from this coincidence unit forms the VETO input to another 365 al coincidence unit. This second 365 al will be referred to as the "trigger coincidence unit". Thus if there was no n-fold trigger then the arrival of a veto pulse at the trigger coincidence unit stops the issuance of triggers to other modules, e.g. common stop to TDCs, list sequencer and GPS clock.

24. This is the output for the Common Stop to the TDCs. It is fed through a channel of the 429f (logic fan-in, fan-out) to copy the signal for the VULCAN trigger. The common stop pulse is then passed through a 4616 NIM-ECL-NIM level translator to convert the input pulse from NIM level to ECL level.
25. The TDC common stop is daisy chained between the TDCs. It is imperative to realise that the TDC calibration was carried out with these modules daisy chained. If this is changed then it will result in differing delays between each TDC and thus lead to misleading time delays being used.
26. This output is passed to a gate generator and delay module (NIM 222) which generates a gate of duration 1 msec. The output from this module is then passed to a 429f (logic fan-in fan-out) module operating in 1x16 mode to produce 16 copies of the input signal.
27. Ten copies of the signal produced by the 429f described above are used to inhibit discriminators. This is to prevent further triggers occurring before the present event has been dealt with.
28. Eight copies of the signal produced by the 429f described above are distributed to the 3412 (D1) discriminators whilst the remaining two are passed to the 4413 (D2) discriminators.
29. This is a NIM level pulse to latch the Leeds GPS clock.
30. This is a NIM level pulse to latch the Webb clock.
31. This is the SPASE-2 trigger for AMANDA. Before the signal is sent to AMANDA it is first delayed and then passed through a thumper unit. The delay is achieved using a 222 module and currently set at 2 μ sec before being passed to the thumper which amplifies the signal so that a -1 to -2 Volt signal is seen in AMANDA. Note that the delay module and thumper unit are not shown on the trigger diagram.
32. This is the trigger output for the list sequencer. In sending this trigger to the list sequencer to initiate the execution of its pre-programmed instruction set it is vital to ensure it does not try to recover information

from modules which are not in a "ready" state. For this purpose the signal is first passed to a 222 module with a gate width of 500 μ sec. Then the delayed output of this signal is fed to a further 222 with a gate width of 250 nsecs. The TTL level signal output is then used to front panel trigger the list sequencer. Although this is a waste of a 222 channel it was the only way to manufacture the TTL level signal this season.

0.2 VULCAN Trigger Logic

The trigger logic flow chart is shown in figure 0.4 The PMT signal is fed directly into the amplifier via RG 8 50 ohm transmission line cable. RG 174 cable fitted with lemo style connectors are used to distribute the two outputs. The two signals are amplified by a factor of five and one, to produce two signals of high and low gain respectively. These signals are the same in every respect but signal size.

The low gain splitter channel output is distributed to a Flash ADC channel, whilst the high gain channel is fed directly into a NIM LeCroy 428f linear fan-in, fan-out module and the three outputs are used in the following ways:

- One signal is fed directly into the Flash ADC for immediate waveform digitisation.
- The second copy is fed into a CAMAC 3412 LeCroy discriminator whose threshold is set at -15 mV and operated in the burst guard mode of operation. A differential ECL level signal is then sent to a CAMAC 4434 LeCroy Scalar (no load or hardware fast clears are issued to this latching scalar) and another copy is also distributed to a multi-hit (both leading and trailing edges) CAMAC 2277 LeCroy TDC. Operating the discriminator in burst guard mode effectively means that the TOT is also known because the TDC registers leading and trailing edges.
- The third output is further amplified by a factor of 20 using a NIM 611L LeCroy PMT amplifier. The output is then discriminated using a CAMAC 3412 LeCroy module at various thresholds. The output from this discriminator is then converted from ECL to NIM level signals utilising a 4616 ECL-NIM-ECL LeCroy level translator and the NIM level signal is then input to a CAMAC 2551 LeCroy scalar. The rate is monitored over a period of a time for a given threshold. This is to study fluctuations in the background sky noise.

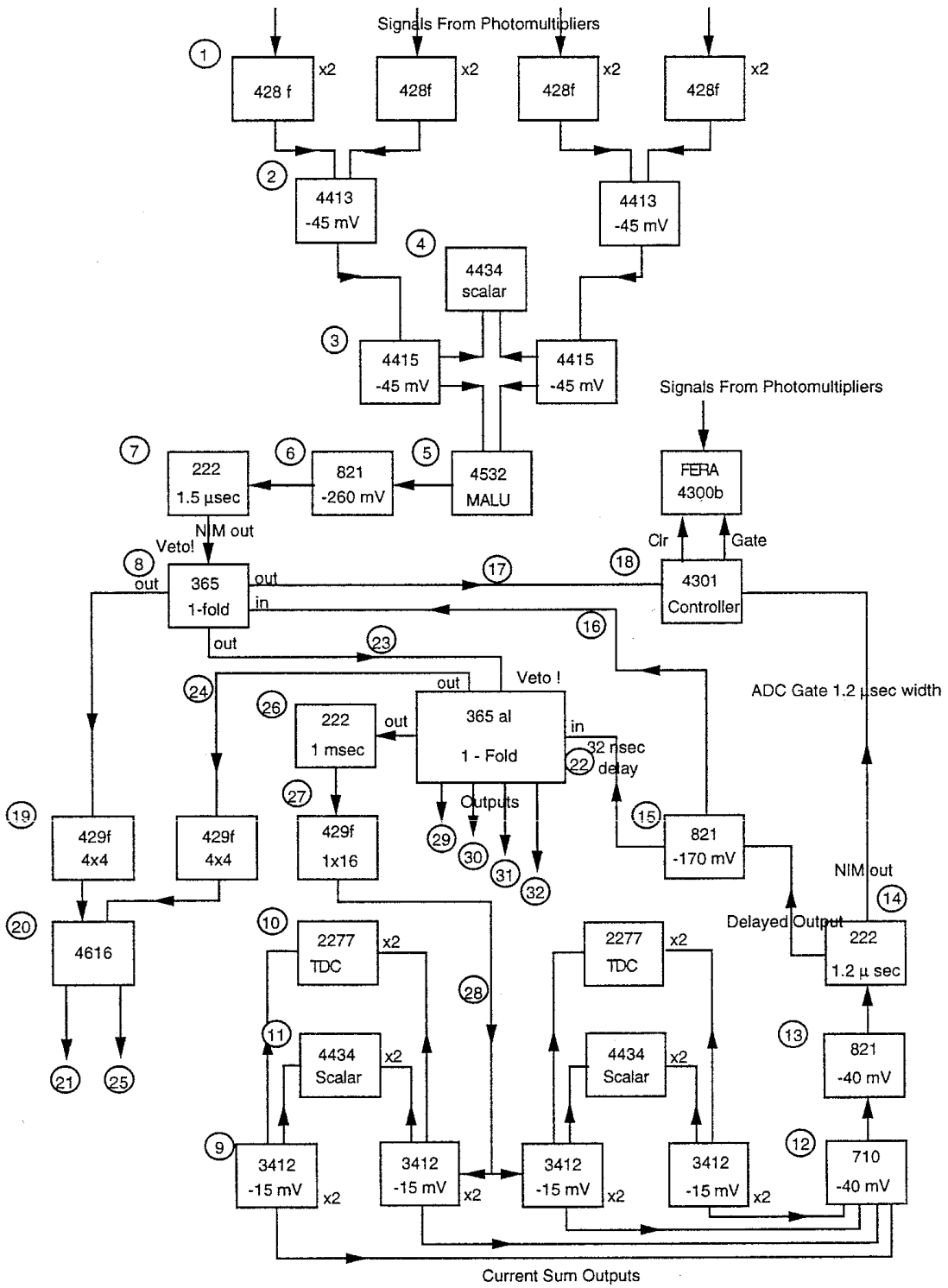


Figure 0.3: SPASE-2 trigger, February 1996

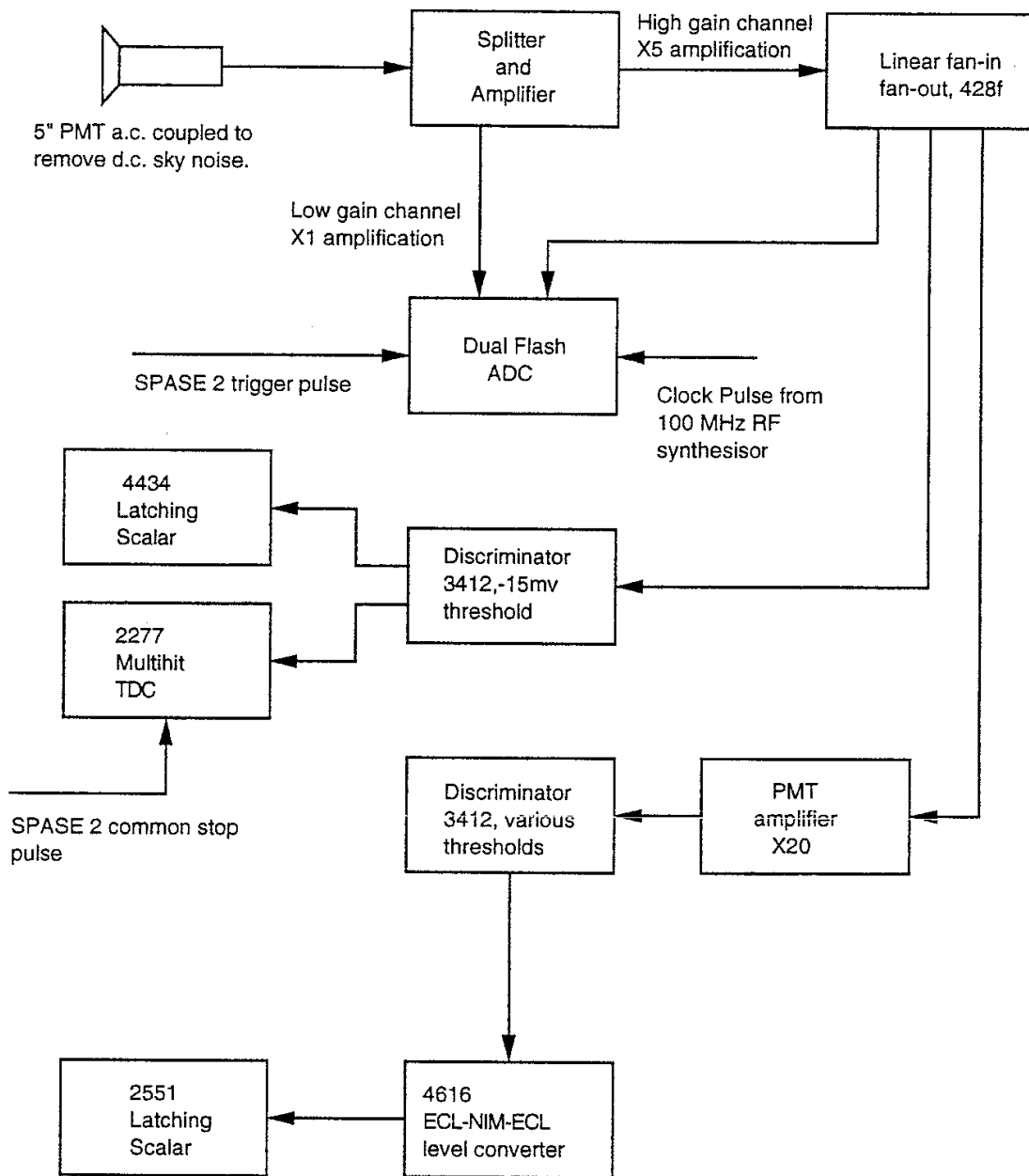


Figure 0.4: VULCAN Trigger Logic Flow chart.